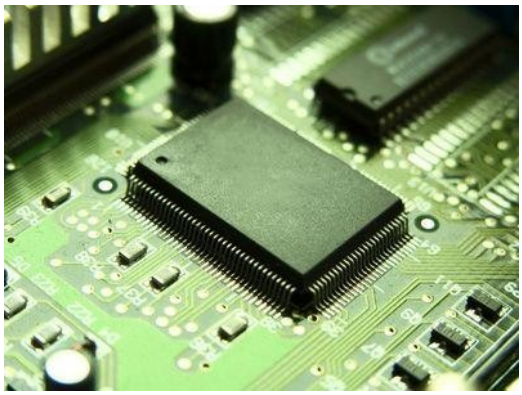
INSTITUTO FEDERAL
São Paulo
Câmpus Campinas

DIG IC Design



FINEP CNPq Facti Centro de Tecnologia da Informação Renato Archer cadence MCTI Ministério da Ciência, Tecnologia e Inovação

1. GENERAL DATA

Course: Digital IC Design	**Code : DB01**
Workload : 40 hours Theorical Lectures **20 hours tutor classes**	**Period : semester I/II / YEAR**
Professor: Daniel De Lárazi	**Contact :**
Main Topics: Introduction to Architecture Styles, Random Logic Architecture, Micro-coded architecture, Bit-Sliced Architecture, Pipeline Architecture, Cache and Virtual Memory, Architectural Exploration and Validation and Architectural Tradeoffs.	

2. OBJETIVES

SCOPE	DESCRIPTION
General	Develop the fundamental analysis of microprocessor architecture and the factors influencing the design of hardware and software elements of computer systems.
Specific	• Microprocessor architecture history, instruction set design, random-logic microprocessor; • Micro-coded microprocessor; pipelined microprocessor, introduction to performance analysis; • Cache hierarchies; • Virtual memory organizations.

3. CONTEXT and MOTIVATION

This course provides the trainee basic concepts of how computer systems are organized and why they are organized that way. They will know the characteristics of modern microprocessors that affect system architecture. These trainees will then be able to design random-logic, micro-coded and pipelined microprocessors and articulate the advantages and disadvantages of the various architecture styles.

The Professor is going to work together with the instructors, whom develop and guide two important activities:

1) They are going to coordinate the lesson, a complementary class which is going to take up to 4 hours per week, in which several practical examples, book problems and homework activities are going to be explained.

2) The Instructors assign to the trainee's practical design activities in order to be developed inside the laboratories. These activities are related to both the actual topic that is being studied in the theoretical lessons and to the EDA tools that the trainee learns.

4. PROGRAM

CLASS ISSUE	DESCRIPTION
1. Introductory concepts of Architecture Styles	Computer architecture: past and present 1.2. Overview of microprocessor architectures
2. Random Logic Architecture	2.1. CPU architecture 2.2. CPU instruction cycle 2.3. Random logic architecture implementation
3. Micro-Coded Architecture	3.1. Review of CPU architecture 3.2. What is micro-coded architecture 3.3. Micro-Code architecture implementation in hardware 3.4. Design considerations
4. Bit-Sliced Architecture	4.1. Historical reasons behind bit-sliced architecture development 4.2. The bit-slice architecture/operand slice 4.3. ALU architectures of 1,2,5 and 8 bits 4.4. Combining smaller bit-width ALU architectures to create large ALU processors 4.5. Description of micro-sequencer or control ROM
5. Pipelined Architecture	5.1. Introduction to the pipelined architecture 5.2. Multiple-Stage pipeline architecture 5.3. Pipeline visualization 5.4. Design and challenges of pipeline architectures 5.5. Data Hazards 5.6. Instruction flow with data forwarding 5.8. Control hazard 5.9. Branch penalty 5.10. Reducing and Control hazard 5.11. Structural hazard.
6. Cache and Virtual Memory	6.1. Memory hierarchy 6.2. Cache system 6.3. Types of cache 6.4. Cache write policy 6.5. L1/L2 cache performance example 6.6. Virtual and Physical memory
7. Validation of Architecture	7.1. Overview and history 7.2. Different methods for validation 7.3. System example 7.4 Mixed simulations with various architectural tradeoffs, etc. 7.5 Flow into real implementation as a system gets micro-architected, then Implemented 7.6 Reuse of testbenches, etc.
8. Architectural Tradeoffs	8.1. Review of CPU architectures 8.2. Detailed implementation tradeoffs and Requirements 8.3 Device 8.4 Process technology

5. ACTIVE SCHEDULE

WEEK	Main Topic	Homework	Tool	Labs ex.
1	**Microcoded Architecture**	Implement a complex instruction using microcode	BP	Code and *testbench* of the BP blocks
2	**Pipelined Architecture**	Identify potential hazards in pipeline.	BP	Labs: Compile BP blocks
3	**Cache and Virtual Memory**	Calculate the missing data fields, to Cover the different mapping techniques for caches.	INC SIM	Labs: simulating and debugging design
4	**Architectural Exploration and Validation**	---	INC SIM Verilog	Labs: Display Driver Components
5	**Architectural Exploration and Validation**	---	Verilog	Labs: Display Driver Components
5	**Formal Study Group Presentation and Final Exam**	Study to formal presentation and final Exam.	Verilog	Labs: Display Driver Components

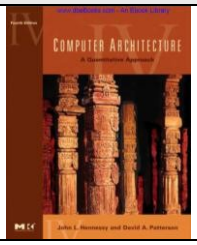
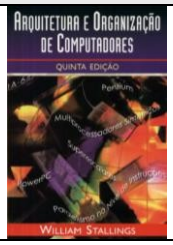
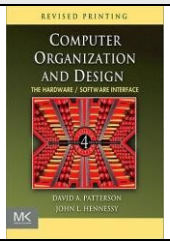
6. EVALUATION SYSTEM

The set of activities to be proposed for evaluating trainee performance are described as follows:

EVALUATON	DESCRIPTION
Homeworks (H)	• Theoretical activity to be developed at home through the application of the concepts presented in the class.
Formal Presentation (FP)	• Individual presentation based on a given topic to be provided during the course.
Final Exam (FE)	• Theoretical verification of the acquired knowledge.

Final Grade (FG)	• **P1 - Home works (40%)** • **P2 - Formal Presentation (15%)** • **P3 - Final Exam (45%)**
	Final grade will be determined through the following expression: • **FG = P1*H + P2*FP + P3*FE**

7. BIBLIOGRAPHY

SOURCE	**Digital Books**				
Library					
	Title: Computer Architecture **Author:** John L. and David A. Patterson	**Title:** Arquitetura e Organização de Computadores **Author:** Willian Stallings	**Title:** Computer Organization and Design **Author:** John L. and David A. Patterson		